CLAIMS

1. A semiconductor device comprising :-

a substrate;

at least one data storage cell provided on one side of said substrate, wherein the or each said data storage cell comprises a respective field effect transistor comprising: (i) a source; (ii) a drain; (iii) a body arranged between said source and said drain and adapted to at least temporarily retain a net electrical charge generated in said body such that the magnitude of said net charge can be adjusted by input signals applied to said transistor; and (iv) at least one gate adjacent said body; and

charge adjusting means for at least partially cancelling the adjustment of said net electrical charge by said input signals, by applying first predetermined electrical voltage signals between at least one corresponding said gate and the corresponding said drain and between the corresponding said source and said drain.

2. A device according to claim 1, wherein said input signals comprise second predetermined electrical voltage signals applied between at least one corresponding said gate and the corresponding said drain and between the corresponding said source and said drain.

3. A device according to claim 2, wherein the device is a memory device.

4. A device according to any one of the preceding claims, wherein the device is a sensor and the charge stored in at least one said body in use represents a physical parameter.

5. A device according to any one of the preceding claims, wherein said input signals comprise electromagnetic radiation.

6. A device according to claim 5, wherein the device is an electromagnetic radiation sensor.

7. A device according to any one of the preceding claims, further comprising a first insulating layer at least partially covering said substrate, wherein the or each said data storage cell is provided on a side of said first insulating layer remote from said substrate.

8. A device according to claim 7, wherein said first insulating layer comprises a layer of semiconductor material of opposite doping type to the body of the or each said data storage cell.

9. A device according to any one of the preceding claims, further comprising a respective second insulating layer provided between at least one said body and the or each corresponding said gate.

10. A device according to claim 9, wherein at least one said transistor includes a plurality of defects in the vicinity of the interface between at least one corresponding said body and the corresponding said second insulating layer, for trapping charge carriers of opposite polarity to the charge carriers stored in the body.

11. A device according to claim 10, wherein the density of defects in the vicinity of said interface is between 10^9 and 10^{12} per cm^2.

12. A device according to any one of the preceding claims, further comprising data reading means for causing an electrical current to flow between a said source and a said drain of at least one said data storage cell by applying third predetermined electrical voltage signals between at least one corresponding said gate and said drain and between said source and said drain.

13. A device according to any one of the preceding claims, wherein said first insulating layer comprises a plurality of insulating layers.

14. A device according to any one of the preceding claims, wherein at least one said data storage cell is adapted to store at least two distinguishable levels of said electrical charge.

15. A device according to claim 14, wherein at least one said data storage cell is adapted to store at least three distinguishable levels of said electrical charge.

16. A device according to any one of the preceding claims, wherein at least one said transistor has a drain/body capacitance greater than the corresponding source/body capacitance.

17. A device according to claim 16, wherein the body of at least one said transistor has a higher dopant density in the vicinity of said drain than in the vicinity of said source.

18. A device according to claim 16 or 17, wherein the area of the interface between the drain and body of at least one said transistor is larger than the area of the interface between the source and the body.

19. A device according to any one of the preceding claims, wherein common source and/or drain regions are shared between adjacent transistors of said device.

20. A method of storing data in a semiconductor device comprising a substrate, and at least one data storage cell provided on one side of said substrate, wherein the or each said data storage cell comprises a respective field effect transistor comprising (i) a source; (ii) a drain; (iii) a body arranged between said source and said drain and adapted to at least temporarily retain a net electrical charge generated in said body such that the magnitude of said net charge can be adjusted by input signals applied to said transistor; and (iv) at least one gate adjacent said body; the method comprising the steps of:

applying first predetermined electrical voltage signals between at least one corresponding said gate and the corresponding said drain and between the corresponding said source and said drain to at least partially cancel the adjustment of said net charge by said input signals.

21. A method according to claim 20, further comprising the step of applying second predetermined electrical voltage signals between at least one said gate of a said data storage cell and the corresponding said drain and between the corresponding said source and said drain.

22. A method according to claim 21, wherein the step of applying second predetermined said electrical signals adjusts the charge retained in the corresponding said body by means of the tunnel effect.

23. A method according to claim 22, wherein the charge is adjusted by the application of a voltage signal between at least one said gate and the corresponding drain such that at the interface between the corresponding body and the drain, the valence and conduction bands of the body and drain are deformed to inject electrons from the valence band to the conduction band by the tunnel effect, causing the formation of majority carriers in the body.

24. A method according to claim 22 or 23, wherein said charge is adjusted by means of tunnelling of electrons from the valence band to at least one gate of a said field effect transistor.

25. A method according to any one of claims 20 to 24, wherein the step of applying first predetermined said voltage signals comprises applying electrical voltage signals between at least one said gate and the corresponding said drain such that at least some of the charge carriers stored in the corresponding body recombine with charge carriers of opposite polarity in said body.

26. A method according to claim 25, further comprising the step of applying at least one said voltage signal comprising a first part which causes a conducting channel to be formed between the source and the drain, the channel containing charge carriers of opposite polarity to the charge carriers stored in said body, and a second part which inhibits formation of the channel, and causes at least some of said stored charge carriers to migrate towards the position previously occupied by said channel and recombine with charge carriers of opposite polarity previously in said channel.

27. A method according to claim 26, further comprising the step of repeating the step of applying at least one said voltage signal in a single charge adjustment operation sufficiently rapidly to cause at least some of said charge carriers stored in the body to recombine with charge carriers of opposite polarity before said charge carriers of opposite polarity can completely migrate to said source or said drain.